REMARKS

Claims 1 – 12, 14 – 23 and 25 - 27 remain in the application. Claims 13, 24 and 28 – 40 are canceled herein. Claims 13 and 24 are objected to for depending from rejected base claims, but were indicated to be allowable if rewritten in independent form. New claims 41 – 55 are presented herein. Claims 1 and 14 are amended herein. No new matter is added. The rejection of the claims is respectfully traversed.

The restriction requirement having been made final, withdrawn claims 28 – 40 are canceled without prejudice herein. New claims 40 – 55, drawn the elected invention, are supported by the claims as filed and the specification and are, in fact, objected to and canceled claims 13 and 24 rewritten in independent form as new claims 41 and 49. Accordingly, new claims 40 – 55 are deemed allowable.

Claims 1 – 16 are rejected under 35 U.S.C. §112 as being indefinite. In particular, the examiner did not understand "lateral extension contact said portions" and "gate said portions" and found no antecedent basis for "said lateral extension contact portions." While the applicants believe that "lateral extension contact said portions" and "gate said portions" adequately refer to "**portions** of a low resistance material layer disposed on said **gate** and [to horizontal surfaces] on said source/drain **extension**" (emphasis added) and so, are definite; rather than belabor this, claim 1 has been amended. Further, the amendment to claim 1 has provided a clear antecedent basis for "said lateral extension contact portions." Claim 14 is amended to provide antecedent basis for the claim. The amendment to claims 1 and 14 is not believed to be restrictive or to further limit the claims. Reconsideration and withdrawal of the rejection of claims 1 – 16 under 35 U.S.C. §112 as being indefinite is respectfully solicited.

Claims 1 – 5, 10 – 12, 14, 16 – 19, 22, 23, 25 and 27 are rejected under 35 U.S.C. §102(b) over U.S. Patent No. 4,788,160 to Havemann et al. Claims 6 – 9, 15, 20, 21 and

26 are rejected under 35 U.S.C. §103(a) over Havemann et al. in view of U.S. Patent No. 4,876,213 to Pfeister and U.S. Patent No. 6,608,354 B2 to Hokazono et al. The rejection is respectfully traversed.

The Examiner asserts that claims 1 – 5, 10 – 12, 14, 16 – 19, 22, 23, 25 and 27 are shown in Havemann et al. by a "field effect transistor comprising a device channel (20), a gate (18), a doped extension (24 or 26), and low resistance material (30, 32, and 24)." For the "source/drain extension has a lateral thickness of less than 100Å thick" as recited in claim 2, for example, the Examiner asserts that "line 55 of column 6 of Havemann [teaches] that the extension has a lateral thickness of approximately 100 angstroms. Note that 'approximately 100 angstroms' can be less than 100Å." Applicants note that Haveman et al. and Pfeister were both initially filed in 1987 – 8, a time frame when a typical CMOS process was based on a 1 micron feature (e.g., minimum channel length) and lightly doped drain (LDD) was initially used to connect the source/drain regions to channels.

Haveman et al. teaches an LDD bulk FET technology, thus, the formation of the sidewall oxide 22 in Figures 2 – 6. These sidewalls are 300Å. See col. 3, lines 59 – 66. What Haveman et al. refers to as "source/drain extension **implants** 24 and 26" are intermediate implants. (emphasis added) *See, e.g.*, Figs. 2 – 4 and col. 4, line15 – col. 6, line 59. Further, these "source/drain extension **implants** 24 and 26" are spaced away from the channel (laterally) by the 300Å oxide sidewalls 22. During fabrication the Haveman et al. device is annealed to diffuse dopant in the "source/drain extension **implants** 24 and 26" which "forms an n+ region 42 beneath the silicide layer 30 to provide one of the source/drain regions and an n+ region 44 beneath the silicide layer 32 to provide the other of the source/drain regions." Col. 6, lines 55 – 59. Thereafter, remaining portions of the "source/drain extension **implants** 24 and 26" are lightly doped and only remain buried under the sidewalls between the channel and device source/drains 42, 44; and only with the lower end of the sidewalls 22 on and contacting the lateral portions of the lightly doped *unsilicided* region 24 and 26. *See,* Figure 5A, Col. 7, lines

14 – 20. This lightly doped *unsilicided* region 24, 26 between the channel and source/drains 42, 44 of Figure 5A of Haveman et al. adds resistance in the source and drain of the device as described in paragraphs 0005 & 6 of the present application.

The present invention includes a FET with a gate disposed above a device channel and "a doped extension at said each end of said device channel, said doped extension being a source/drain extension" as recited in claim 1, lines 1 – 5. A low resistance material layer (e.g., a silicide layer) on both the gate and the lateral surface of the source/drain extensions reduces gate and source/drain extension resistance. Thus claim 1 further recites "portions on each said source/drain extension providing direct contact with said source/drain extension" and silicide portions on the gate are "separated from said lateral extension contact portions."

Source/drain extensions between a silicided source/drain diffusion and a channel are well known and their formation is described at paragraph 0005 of the present application. These well known source/drain extensions add resistance in series with the silicided source/drain diffusion and the device channel as described in paragraph 0006 of the present application. Previous attempts to silicide these source/drain extensions failed to yield devices because of gate to source/drain and channel spiking shorts as described in paragraph 0007 of the present application. Thus, typically, as recited in paragraph 5, "thick spacers are formed at each end of FET gates. The spacer blocks or attenuates the higher energy deep source/drain dopant implant at the areas adjacent to the gates, spacing the source/drain diffusion regions away from the gate." Thus, the thick, 300Å spacers above the lightly doped *unsilicided* region 24, 26 of Havemann et al. Accordingly, siliciding source/drain extensions is neither shown nor described in any reference of record, nor is one told how to silicide source/drain extensions without silicide spiking shorting the extensions to FET gates. Further since the lightly doped *unsilicided* region 24, 26 of Havemann et al. are at least 300Å long, each source/drain extension could not be 100Å or shorter as recited in claim 2. Therefore, Havemann et al. does not teach the present invention as recited in any of claims 1 – 5, 10 – 12, 14, 16 – 19, 22, 23, 25 and

27. Since Havemann et al. does not teach every element of the present invention as recited in any of claims 1 – 5, 10 – 12, 14, 16 – 19, 22, 23, 25 and 27, Havemann et al. does not teach the present invention under 35 U.S.C. §102(b). Reconsideration and withdrawal of the rejection of claims 1 – 5, 10 – 12, 14, 16 – 19, 22, 23, 25 and 27, under 35 U.S.C. §102(b) over Havemann et al. is respectfully solicited.

Regarding the rejection of claims 6 – 9, 15, 20, 21 and 26 under 35 U.S.C. §103(a) over Havemann et al. in view of Pfeister and Hokazono et al., neither Pfeister nor Hokazono et al. adds anything to Havemann et al. to result in the present invention as claimed in claims 1 – 5, 10 – 12, 14, 16 – 19, 22, 23, 25 and 27, much less in claims 6 – 9, 15, 20, 21 and 26, depending therefrom. Be that as it may, however, the MPEP §2142 provides in pertinent part:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation,... . Second, there **must be a reasonable expectation of success**. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination **and the reasonable expectation of success** must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (emphasis added.)

Thus, to suggest the invention, the references relied upon must show how to overcome the drawbacks described in the present application, i.e., how to silicide source/drain extensions without shorting the extensions to FET gates. Accordingly, Havemann et al. in view of Pfeister and Hokazono et al. fails to overcome the shortfalls inherent in the prior art and is insufficient to establish a *prima facie* case of obviousness. Reconsideration and withdrawal of the rejection of claims 6 – 9, 15, 20, 21 and 26 under 35 U.S.C. §103(a) is respectfully solicited.

The applicants have considered the other references of record and find them to be no more pertinent then the references relied upon in this Office Action.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance for the reasons

set forth above, the applicants respectfully request that the Examiner independently consider new claims 40 – 55, reconsider and withdraw the rejection of claims 1 – 12, 14 – 16, under 35 U.S.C. §112, reconsider and withdraw the rejection of claims 1 – 5, 10 – 12, 14, 16 – 19, 22, 23, 25 and 27, under 35 U.S.C. §102(b), reconsider and withdraw the rejection of claims 6 – 9, 15, 20, 21 and 26 under 35 U.S.C. §103(a) and allow the application to issue.

Should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 09-0458 and advise us accordingly.

Respectfully Submitted,

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(Date)

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